Pendahuluan Pengolahan Paralel

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Lab Embedded, Siskom - Undip

Bahasan

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Pengantar Perkuliahan

Deskripsi Kuliah

Kredit: 2 SKS Kuliah
Waktu: Kamis, 07.50 - 09.30
Metode pengajaran: tatap muka (2 x 50 menit), presentasi materi, diskusi, presentasi proyek
Waktu: ±14 Minggu

Teknik-teknik pemrosesan paralel: konsep sistem komputer paralel, arsitektur, model dan pemrograman paralel untuk aplikasi komputasional

Pemrograman paralel di atas mesin paralel dengan arsitektur memori bersama dan arsitektur memori terdistribusi

Model pemrograman thread untuk mesin memori bersama, yaitu komputer multiprosesor simetrik (SMP,symmetric multiprocessor)

Model pemrograman message passing (MP) untuk mesin memori terdistribusi

Prasyarat: TSK 307 Organisasi Komputer, TSK 401 Arsitektur Komputer

Pokok Bahasan

- Konsep pengolahan paralel: latar belakang kebutuhan, perbandingannya dengan pengolahan serial dalam memecahkan problem komputasional dan faktor speedup (hukum Amdahl) serta taksonomi pengolahan data/instruksi (Flynn);
- Arsitektur komputer paralel, meliputi arsitektur shared memory, distributed dan hybrid;
- Model pemrograman paralel berbasis thread dan message passing serta implementasinya masing-masing di arsitektur komputer paralel;
- Pemrograman paralel di komputer SMP untuk memecahkan problem matematis, misalnya operasi perkalian matrik. Pemrograman paralel menggunakan model thread, baik dengan pustaka POSIX thread (pthread) maupun OpenMP;
- Pemrograman paralel di sistem terdistribusi menggunakan model message passing dengan pustaka MPI (message passing interface);
- Performansi program paralelnya dalam hal speedup terhadap pengolahan serial;

Buku Acuan/Referensi

1. Ananth Grama, "Introduction to Parallel Computing 2nd Edition", 2003
2. David Culler J.P. Singh, "Parallel Computer Architecture: A Hardware/Software Approach", Morgan Kaufmann, 1999
3. 2.Kai Hwang, Zhiwei Xu, "Scalable Parallel Computing: Technology, Architecture, Programming", McGraw Hill, 1998
4. Behrooz Parhami, "Introduction to Parallel Processing: Algorithms and Architectures", Kluwer Academic Publishers, 2002
5. Technical Report No. UCB/EECS-2006-183: The Landscape of Parallel Computing Research: A View from Berkeley
6. Message Passing Interface Forum, “MPI: A Message-Passing Interface Standard v2.2”, 2009
7. Website:
   (a) OpenMP resources: http://openmp.org/wp/resources/. Berisi tutorial, handout dan contoh pemrograman paralel menggunakan OpenMP;
   (b) MPI Official website: http://www.mpi-forum.org/. Berisi dokumen standar dan guide untuk MPI;

Standar Kompetensi

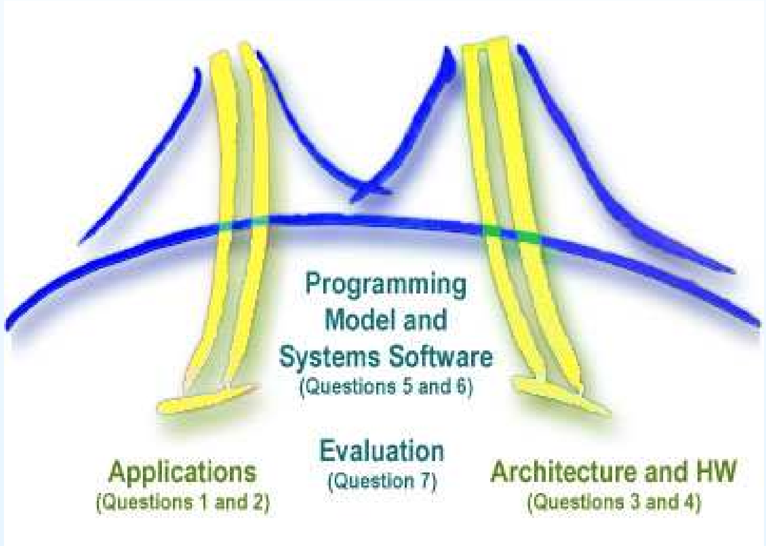
Setelah menyelesaikan pembelajaran kuliah ini, mahasiswa akan mampu mendesain program paralel untuk memecahkan problem-problem matematis menggunakan konsep dan teknik pemrosesan paralel, yaitu:

1. mampu membuat program paralel dengan model thread di sistem komputer SMP menggunakan POSIX thread dan OpenMP;
2. mampu membuat program paralel dengan model message-passing di sistem terdistribusi menggunakan MPI
3. mampu menganalisis faktor speedup yang diperoleh dari program paralel tersebut;

Fokus Kuliah

- The Landscape of Parallel Processing Research: The View from Berkeley (must read)
- 7 Pertanyaan tentang Paralelisme

1. What are the apps?
2. What are kernels of apps?
3. What are the HW building blocks?
4. How to connect them?
5. How to describe apps and kernels?
6. How to program the HW?
7. How to measure success?



TSK-617 berfokus ke pertanyaan 6 dan 7

The Landscape of Parallel Processing

- Spektrum komputing: Embedded - HPC (now)
  - Keduanya konsen ke power
  - Keduanya konsen utilisasi hardware. Sensitif ke biaya: penggunaan hardware yang efisien akan diperlukan
  - Keduanya networked
  - Perbedaan:
    - Embedded: hard-realtime, *guaranted-worst case*. Program harus cukup cepat untuk memenuhi deadline. Tidak ada benefit untuk run lebih cepat
    - HPC: Kecepatan akan sangat berharga
- Pergeseran paradigma
  - Old: Mempercepat frekuensi merupakan metode utama untuk meningkatkan performansi prosesor
  - New: Menambah paralelisme sebagai metode utama

Sistem Evaluasi

Evaluasi:

No	Evaluasi	Bobot
1	Tugas, Paper, Presentasi	20%
2	Ujian Tengah Semester / Take-Home Test	40%
3	Ujian Akhir Semester / Tugas Project	40%

- Tugas berupa penulisan review makalah ilmiah terkait arsitektur paralel. Tugas memprogram paralel suatu rutin
- UTS berisi evaluasi pemahaman konsep dasar pengolahan paralel
- Project tim mengevaluasi kemampuan pemahaman teknik untuk mendesain, mengimplementasikan dan mengevaluasi program paralel
  - Ide project (boleh dari mahasiswa, dengan persetujuan dosen)
  - Hasilnya dipresentasikan dengan jadwal <tbd>
- Paperless, web personal

Pendahuluan Pengolahan Paralel

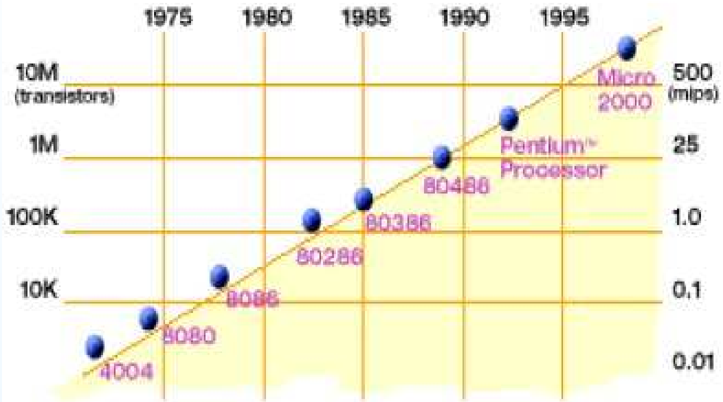
Pembahasan

- Mengapa semua komputer harus paralel?
  - Termasuk laptop dan perangkat handheld

Unit Pengukuran

- High Performance Computing (HPC) units are:
  - Flop: floating point operation, usually double precision unless noted
  - Flop/s: floating point operations per second
  - Bytes: size of data (a double precision floating point number is 8)
- Typical sizes are millions, billions, trillions. . .
  - Mega Mflop/s = 10^6 flop/sec Mbyte = 220 = 1048576 ~ 106 bytes
  - Giga Gflop/s = 10^9 flop/sec Gbyte = 230 ~ 109 bytes
  - Tera Tflop/s = 10^{12} flop/sec Tbyte = 240 ~ 1012 bytes
  - Peta Pflop/s = 10^{15} flop/sec Pbyte = 250 ~ 1015 bytes
  - Exa Eflop/s = 10^{18} flop/sec Ebyte = 260 ~ 1018 bytes
  - Zetta Zflop/s = 10^{21} flop/sec Zbyte = 270 ~ 1021 bytes
  - Yotta Yflop/s = 10^{24} flop/sec Ybyte = 280 ~ 1024 bytes
- Current fastest (public) machine ~ 4.7 Pflop/s
  - Up-to-date list at www.top500.org

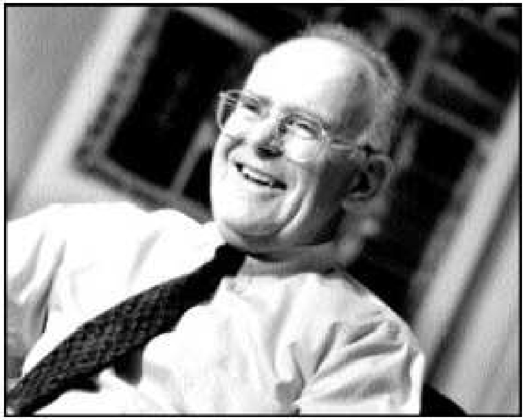
Trend Teknologi: Kapasitas Mikroprosesor



2X transistors/Chip Every 1.5 years

Called "Moore's Law"

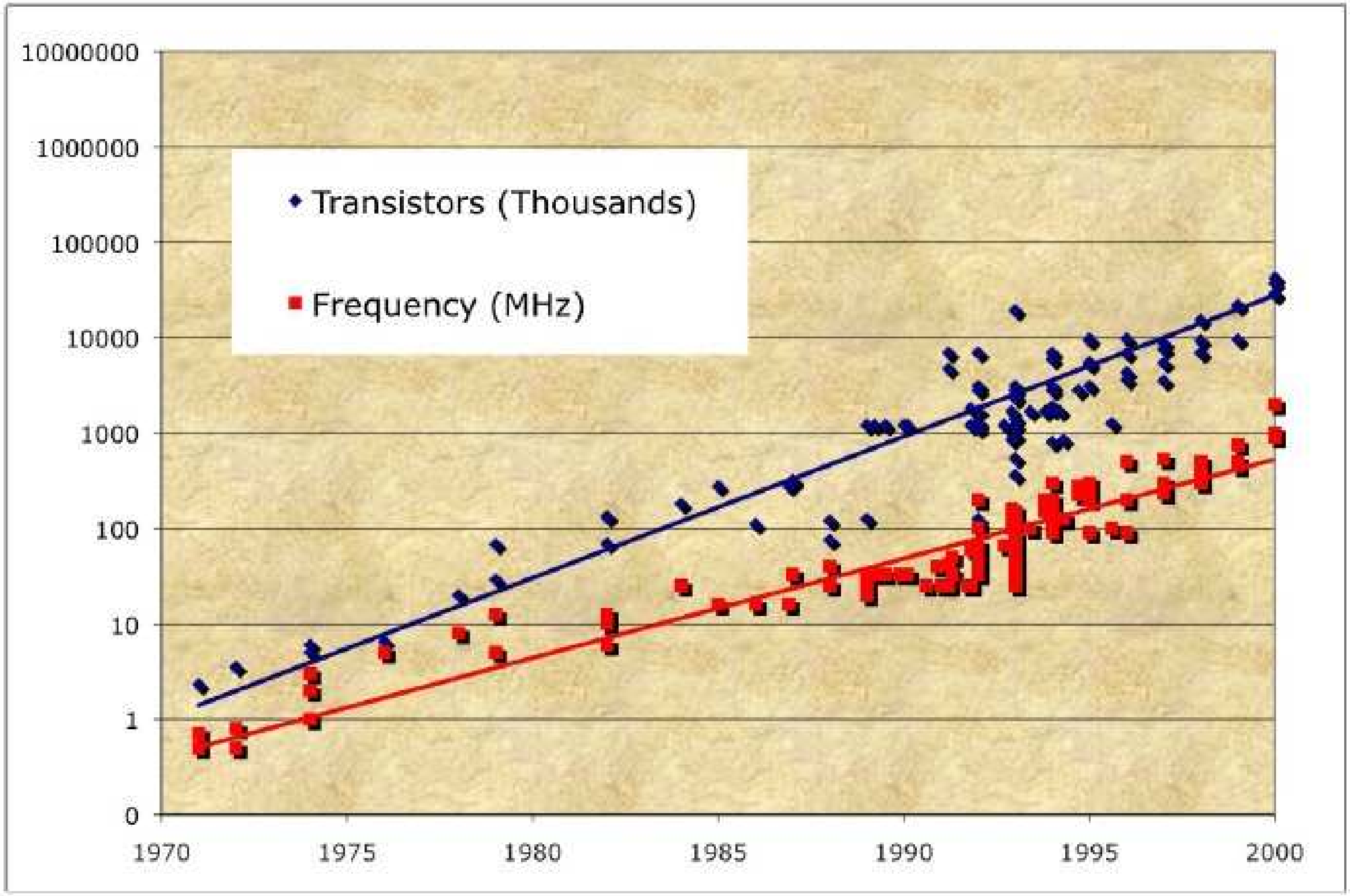
Microprocessors have become smaller, denser, and more powerful.



Gordon Moore (co-founder of Intel) predicted in 1965 that the transistor density of semiconductor chips would double roughly every 18 months.

Slide source: Jack Dongarra

Transistor Mikroprosesor / Clock (1970-2000)

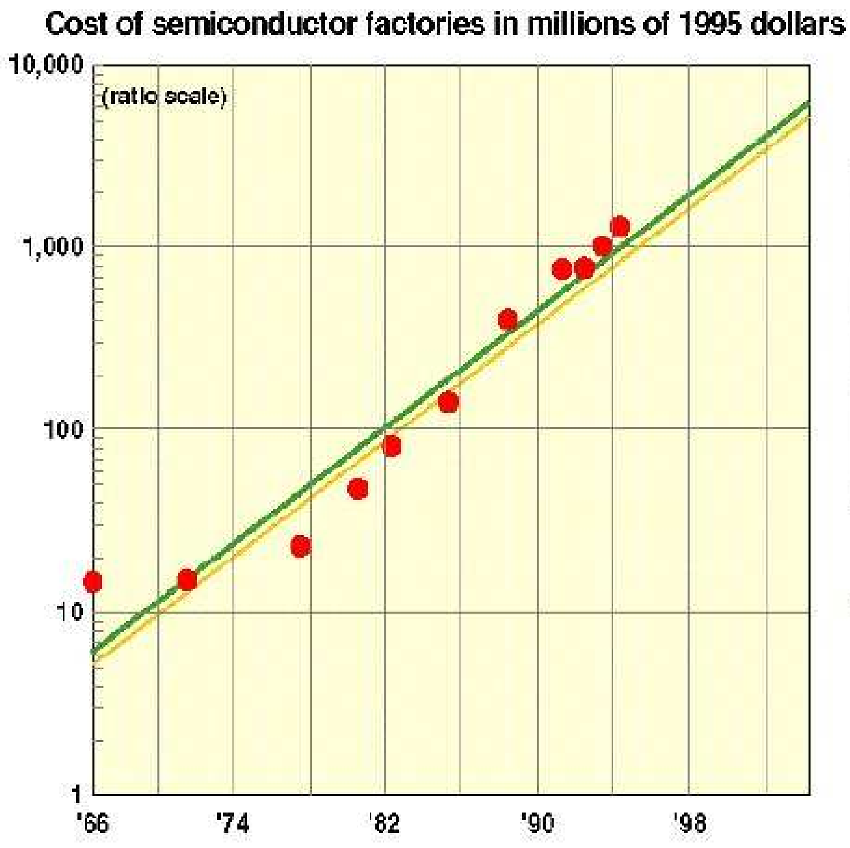


Pengaruh Pertambahan Densitas Transistor

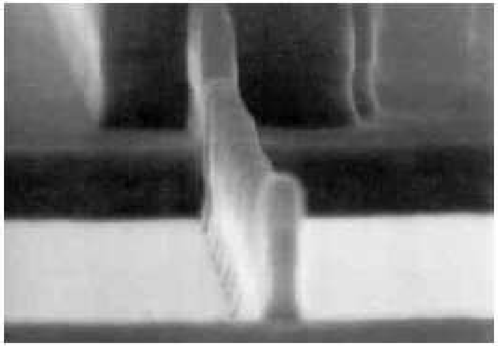
- What happens when the feature size (transistor size) shrinks by a factor of x?
- Clock rate goes up by x because wires are shorter
  - actually less than x, because of power consumption
- Transistors per unit area goes up by x^2
- Die size also tends to increase
  - typically another factor of ~x
- Raw computing power of the chip goes up by ~ x^4 !
  - typically x^3 is devoted to either on-chip
    - parallelism: hidden parallelism such as ILP
    - locality: caches
- So most programs x^3 times faster, without changing them

Isu Manufaktur: Membatasi Performansi

- Manufacturing costs and yield problems limit use of density



- Moore's 2nd law (Rock's law): costs go up



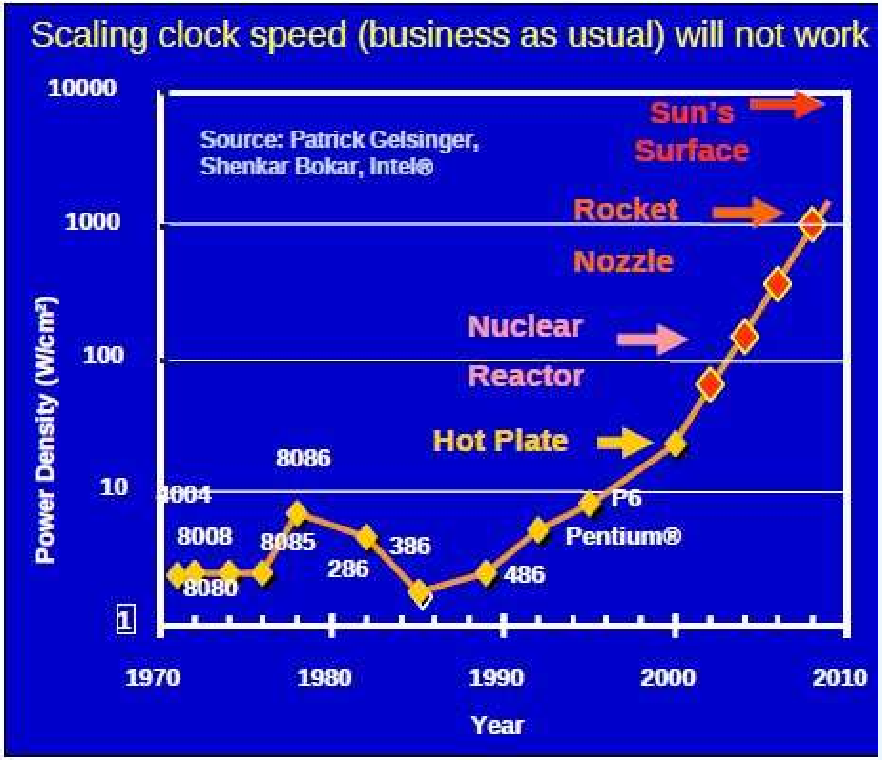
Demo of 0.06 micron CMOS

Source: Forbes Magazine

- **Yield**
  - -What percentage of the chips are usable?
  - -E.g., Cell processor (PS3) is sold with 7 out of 8 "on" to improve yield

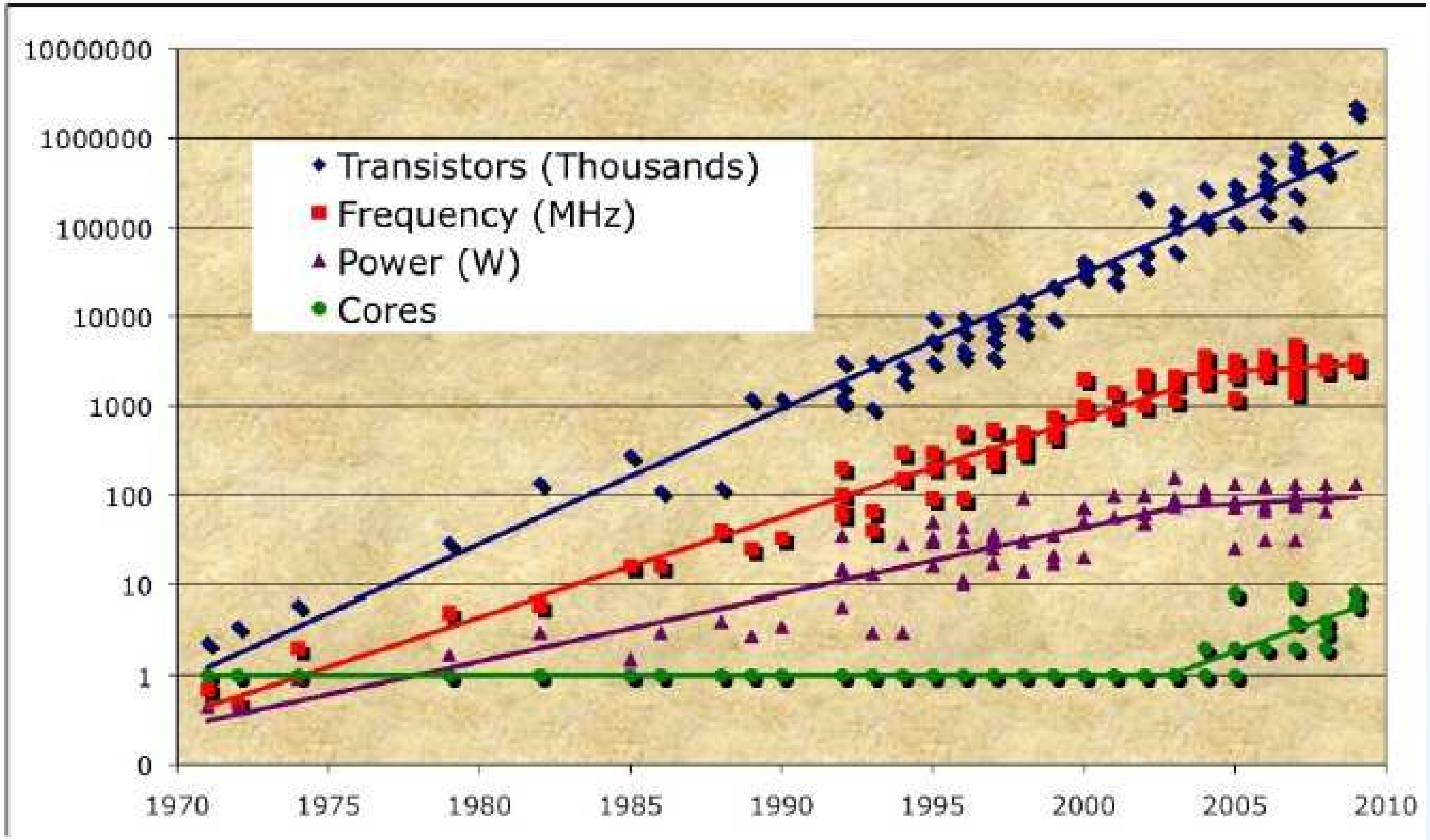
Densitas Power Membatasi Performansi Prosesor Serial

- Concurrent systems are more power efficient
  - Dynamic power is proportional to V^2fC
  - Increasing frequency (f) also increases supply voltage (V) → cubic effect
  - Increasing cores increases capacitance (C) but only linearly
  - Save power by lowering clock speed



- High performance serial processors waste power
  - Speculation, dynamic dependence checking, etc. burn power
  - Implicit parallelism discovery
- More transistors, but not faster serial processors

Revolusi di Prosesor



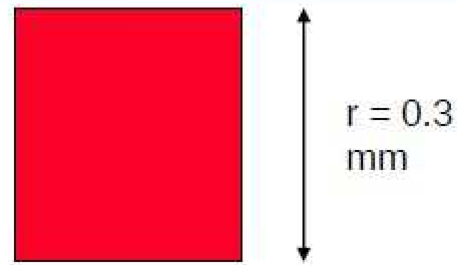
- Chip density is continuing increase ~2x every 2 years
- Clock speed is not
- Number of processor cores may double instead
- Power is under control, no longer growing

Paralelisme di Tahun 2011?

- These arguments are no longer theoretical
- All major processor vendors are producing multicore chips
  - Every machine will soon be a parallel machine
  - To keep doubling performance, parallelism must double
- Which commercial applications can use this parallelism?
  - Do they have to be rewritten from scratch?
- • Will all programmers have to be parallel programmers?
  - New software model needed
  - Try to hide complexity from most programmers – eventually
  - In the meantime, need to understand it
- Computer industry betting on this big change, but does not have all the answers

Seberapa Cepat Komputer Serial?

1 Tflop/s, 1 Tbyte sequential machine



- Consider the 1 Tflop/s sequential machine:
  - Data must travel some distance, r, to get from memory to processor.
  - To get 1 data element per cycle, this means 10^{12} times per second at the speed of light, $c = 3x10^8$ m/s. Thus $r < c/10^{12} = 0.3$ mm.
- Now put 1 Tbyte of storage in a 0.3 mm x 0.3 mm area:
  - Each bit occupies about 1 square Angstrom, or the size of a small atom.
- No choice but parallelism

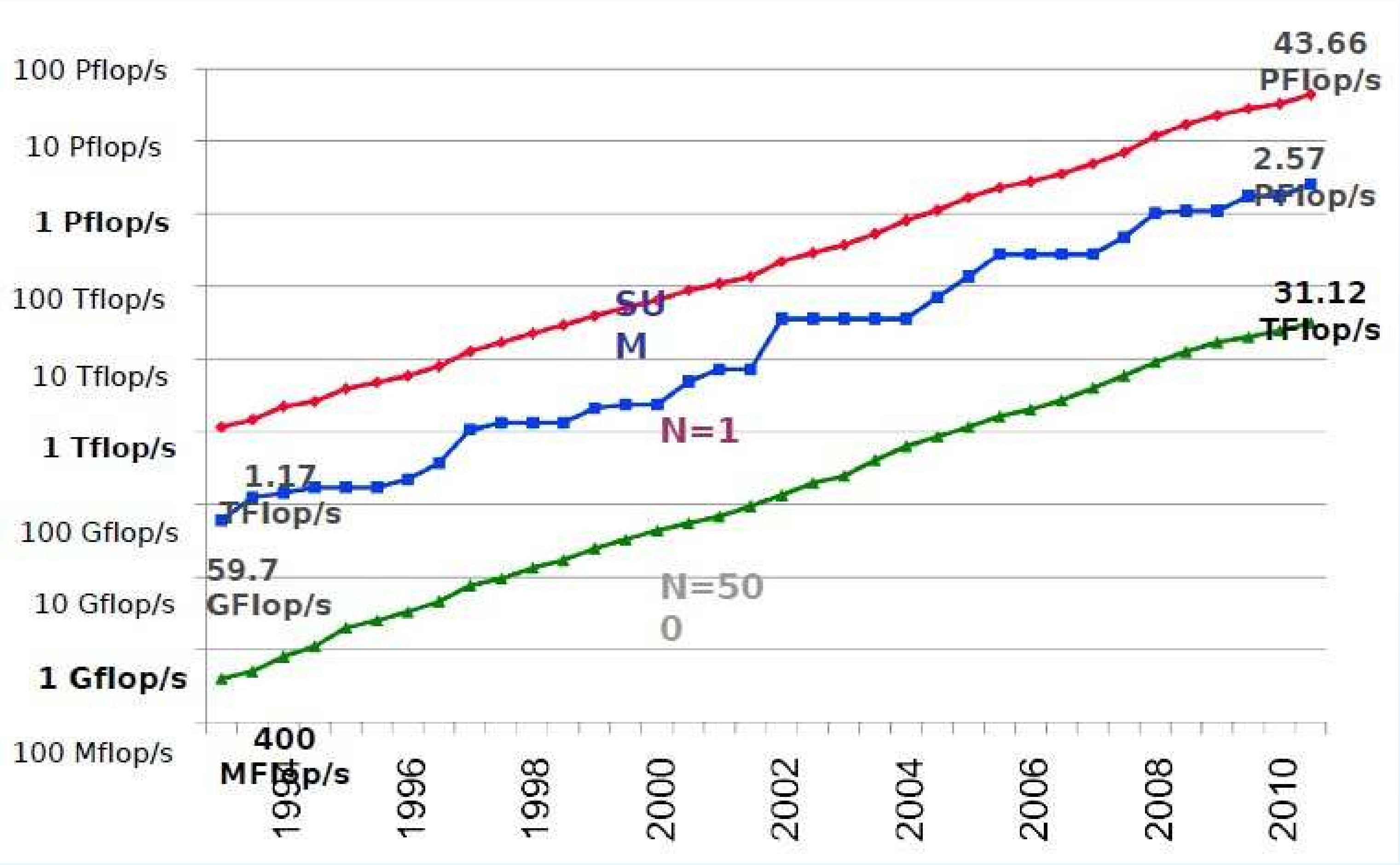
Project TOP500

- Listing the 500 most powerful computers in the world
- Yardstick: Rmax of Linpack
  - Solve Ax=b, dense problem, matrix is random
  - Dominated by dense matrix-matrix multiply
- Update twice a year:
  - ISC'xy in June in Germany
  - SCxy in November in the U.S.
- All information available from the TOP500 web site at: www.top500.org

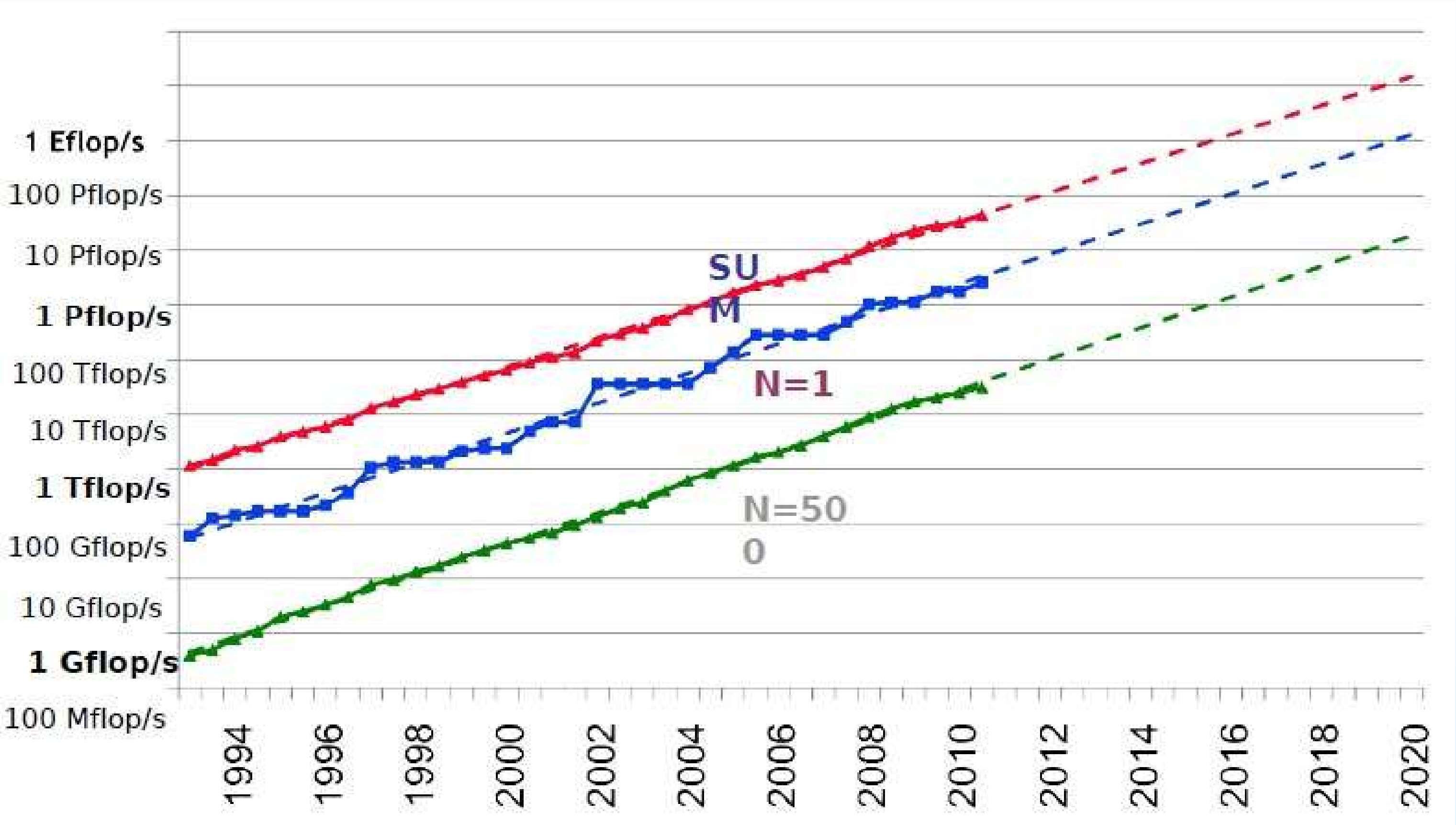
List-36: Top10

Rank	Site	Manufacturer	Computer	Country	Cores	Rmax [Tflops]	Power [MW]
1	National SuperComputer Center in Tianjin	NUDT	Tianhe-1A NUDT TH MPP, Xeon 6C, NVidia, FT-1000 8C	China	186,368	2,566	4.04
2	Oak Ridge National Laboratory	Cray	Jaguar Cray XT5, HC 2.6 GHz	USA	224,162	1,759	6.95
3	National Supercomputing Centre in Shenzhen	Dawning	Nebulae TC3600 Blade, Intel X5650, NVidia Tesla C2050 GPU	China	120,640	1,271	2.58
4	GSIC, Tokyo Institute of Technology	NEC/HP	TSUBAME-2 HP ProLiant, Xeon 6C, NVidia, Linux/Windows	Japan	73,278	1,192	1.40
5	DOE/SC/ LBNL/NERSC	Cray	Hopper Cray XE6, 6C 2.1 GHz	USA	153,408	1.054	2.91
6	Commissariat a l'Energie Atomique (CEA)	Bull	Tera 100 Bull bullx super-node S6010/S6030	France	138.368	1,050	4.59
7	DOE/NNSA/LANL	IBM	Roadrunner BladeCenter QS22/LS21	USA	122,400	1,042	2.34
8	University of Tennessee	Cray	Kraken Cray XT5 HC 2.36GHz	USA	98,928	831.7	3.09
9	Forschungszentrum Juelich (FZJ)	IBM	Jugene Blue Gene/P Solution	Germany	294,912	825.5	2.26
10	DOE/NNSA/ LANL/SNL	Cray	Cielo Cray XE6, 6C 2.4 GHz	USA	107,152	816.6	2.95

Pengembangan Performansi



Proyeksi Performansi



Hukum Moore: Reintepreted

- Number of cores per chip will double every two years
- Clock speed will not increase (possibly decrease)
- Need to deal with systems with millions of concurrent threads
- Need to deal with inter-chip parallelism as well as intra-chip parallelism