

Antarmuka Bus CPU-Memory dan Memory-mapped I/O

TSK304 - Teknik Interface dan Peripheral

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Teknik Sistem Komputer - Universitas Diponegoro

- ▶ Pembahasan tentang antarmuka bus CPU dan diagram pewaktuan
 - ▶ operasi pembacaan dan penulisan
 - ▶ ruang alamat dan dekoding
 - ▶ pemetaan alamat
 - ▶ contoh desain
- ▶ Referensi:
 - ▶ Ken Arnold, “Embedded Controller Hardware Design”, Bab 5-6, 2000
 - ▶ 8051 SBC,
<http://www.kmitl.ac.th/~kswichit/8051sbc/8051sbc.html>

Antarmuka Bus CPU

Bus Mikrokomputer

Parameter Pewaktuan dan Siklus

Operasi Read dan Write

Bus termultipleks (Von Neuman)

Antarmuka Bus
CPU

Ruang Alamat dan
Dekoding

Contoh Desain

Ruang Alamat dan Dekoding

Ruang Alamat

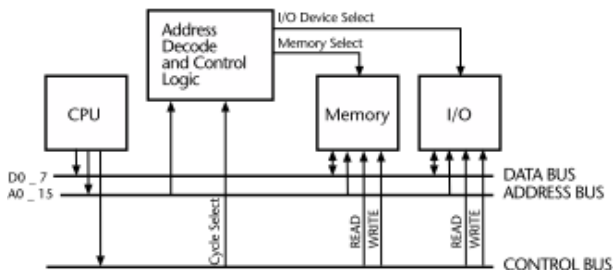
Dekoding Alamat Memori

Dekoding Alamat I/O (Memory-Mapped)

Contoh Desain

Bus Mikrokomputer

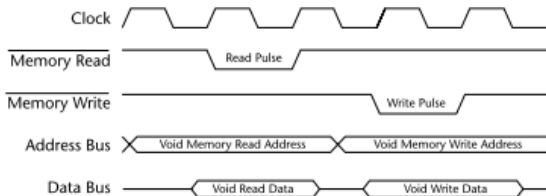
Microcontroller, Control Logic, Memory and I/O



- ▶ Tipe data transfer yang dikontrol CPU:
 - ▶ CPU reads data/instruction from memory (*memory read*)
 - ▶ CPU writes data to memory (*memory write*)
 - ▶ CPU reads data from I/O (*I/O read*)
 - ▶ CPU writes data to I/O (*I/O write*)

Siklus Memori

Operasi Memori General



▶ Memori Read

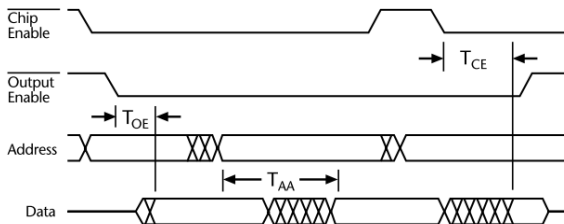
- ▶ Prosesor meletakkan alamat ke bus alamat dan mengaktifkan sinyal read (active-low)
- ▶ Memori meletakkan data sesuai alamat ke bus data

▶ Memori Write

- ▶ Prosesor meletakkan alamat ke bus alamat dan meletakkan data ke bus data dan mengaktifkan sinyal write (active-low)
- ▶ Memori menyimpan data ke alamat yang ditunjuk

Parameter Pewaktuan

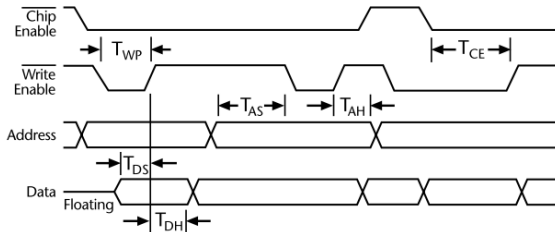
Siklus Memory Read (Memori ke CPU)



- ▶ T_{AA} (*address access time*): Valid Address to valid data delay
- ▶ T_{OE} (*output enable access time*): Output Enable (OE) to valid data delay
- ▶ T_{CE} (*chip enable access time*): Chip Enable (CE) to valid data delay

Parameter Pewaktuan

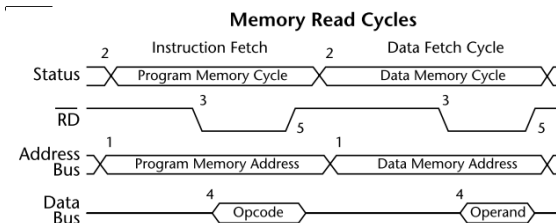
Siklus Memory Write (CPU ke Memori)



- ▶ T_{WP} : Write pulse width
- ▶ T_{AS} : Address setup time
- ▶ T_{AH} : Address hold time
- ▶ T_{DS} : Data setup time
- ▶ T_{DH} : Data hold time

Siklus Pembacaan Memori

- ▶ CPU membaca instruksi (opcode) dan data (operand) dari memori

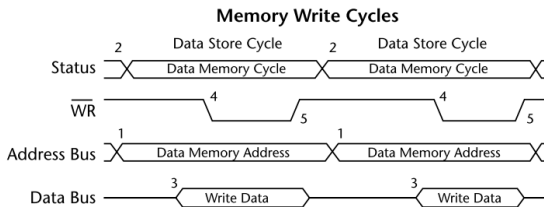


Operasi Siklus Pembacaan Memori

- ▶ The CPU selects the memory location by driving the address on the address bus
- ▶ Control lines are driven by the CPU to indicate the address space to use
 - ▶ such as program memory, data memory, I/O, or special cycles such as interrupts
- ▶ Read is activated on the control bus by the CPU to indicate that the memory can drive the data bus with the contents of the selected location
- ▶ The memory drives the contents of the selected location on the data bus
- ▶ The CPU deactivates the address and control lines, turning off the memory drivers

Siklus Penulisan Memori

- ▶ CPU menulis instruksi (opcode) dan data (operand) ke memori



Operasi Siklus Pembacaan Memori

- ▶ The CPU selects the memory location by driving the address on the address bus
- ▶ Control lines are driven by the CPU to indicate the address space to use
- ▶ The CPU drives the data to be written on the data bus
- ▶ Write is activated on the control bus by the CPU to indicate that the data on the data bus should be written into the selected location
- ▶ The CPU deactivates the address, data, and control lines

Kapasitas dan Bandwidth

- ▶ Bus alamat
 - ▶ Lokasi memori untuk transfer data
 - ▶ Lokasi I/O
- ▶ Lebar bus alamat: 8-bit, 16-bit, 32-bit
 - ▶ Prosesor dengan N-bit alamat, bisa mengalamatkan 2^N lokasi memori
 - ▶ Misalnya: 16-bit alamat bisa mengalamatkan 2^{16} lokasi atau 65.536 (64KB)
- ▶ Lebar bus data menentukan jumlah data yang dapat ditransfer di bus (data throuhtput)
 - ▶ Bus data 8-bit dan periode $T=1\mu s$ (atau $f=1\text{MHz}$), maka untuk satu byte percycle, diperoleh throughtput 1 MBps atau 8 Mbps

Siklus Bus Termultipleks

Di Arsitektur Von Neuman (Princeton)

Antarmuka Bus
CPU-Memory dan
Memory-mapped
I/O

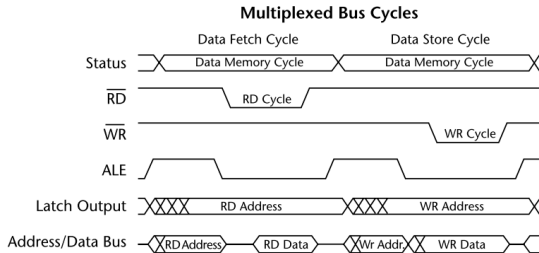
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Antarmuka Bus
CPU

Bus Mikrokomputer
Parameter Pewaktuan dan
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Operasi Read dan Write
Bus termultipleks (Von
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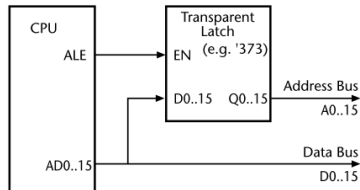
Ruang Alamat dan
Dekoding

Contoh Desain



Address Demux dengan Sebuah Latch

- ▶ Latch: 74xx373 (active high latch)

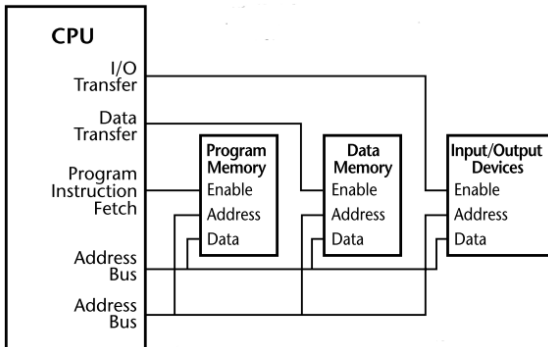


Ruang Alamat

- ▶ Prosesor dapat mempunyai beberapa ruang alamat terpisah:
 - ▶ program memory address space
 - ▶ data memory address space
 - ▶ input/output device address space
 - ▶ stack address space
- ▶ Dapat terpisah maupun overlapping atau satu ruang alamat bersama

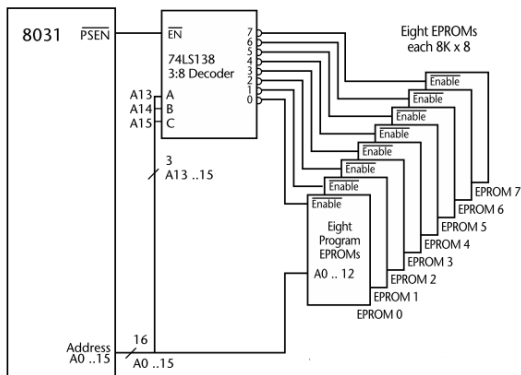
Dekoding Alamat

- ▶ Ruang alamat terpisah untuk memori program, memori data dan device I/O (*memory-mapped*)



Rangkaian Dekoder Alamat

- Mendekodekan jalur alamat dan kontrol untuk menyediakan sinyal Chip Select ke memori dan I/O



Peta Alamat Memori

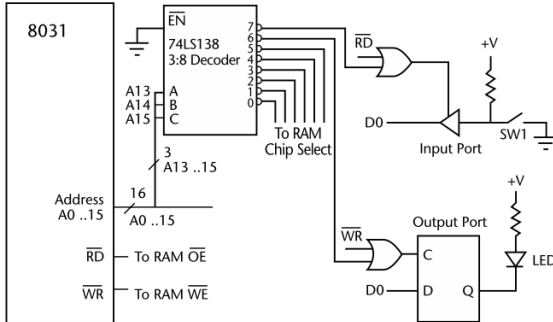
- ▶ Ruang alamat 64KB (16-bit alamat): 8 buah EEPROM 8KB
 - ▶ Tidak ada alamat yang tidak digunakan
 - ▶ Tidak ada duplikasi

Address Range (hex)	Address bits A15 A14 A13	Decoder Outputs 76543210	Chip Select Active for Memory IC
0000 - 1FFF	0 0 0	11111110	EPROM 0
2000 - 3FFF	0 0 1	11111101	EPROM 1
4000 - 5FFF	0 1 0	11111011	EPROM 2
6000 - 7FFF	0 1 1	11110111	EPROM 3
8000 - 9FFF	1 0 0	11101111	EPROM 4
A000 - BFFF	1 0 1	11011111	EPROM 5
C000 - DFFF	1 1 0	10111111	EPROM 6
E000 - FFFF	1 1 1	01111111	EPROM 7

Memory-mapped I/O

Partial Address Decoding

- Pengalamatan memory-mapped I/O untuk switch dan LED



Peta Alamat I/O

Address Range (hex)	Address bits A15 A14 A13	Decoder Ouputs 76543210	Active Select: Memory I/O
0000 - 1FFF	0 0 0	11111110	RAM 0
2000 - 3FFF	0 0 1	11111101	RAM 1
4000 - 5FFF	0 1 0	11111011	RAM 2
6000 - 7FFF	0 1 1	11110111	RAM 3
8000 - 9FFF	1 0 0	11101111	RAM 4
A000 - BFFF	1 0 1	11011111	RAM 5
C000 - DFFF	1 1 0	10111111	Output Port
E000 - FFFF	1 1 1	01111111	Input Port

Single Board Computer 8051

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Antarmuka Bus
CPU

Ruang Alamat dan
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Contoh Desain

Detail.

Lihat project:

<http://www.kmitl.ac.th/~kswichit/8051sbc/8051sbc.html>